

REMARKS

Claims 1 and 3-24 are currently pending in the subject application and are presently under consideration. Claims 1, 4, 5, 7, 10, and 17 have been amended as shown pages 2-5 of this reply. Claims 9 and 15 have been cancelled.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1, 3-8, 10, and 17-23 Under 35 U.S.C. §103(a)

Claims 1, 3-8, 10, and 17-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Singh, *et al.* (US 6,650,422, hereinafter referred to as Singh) in view of Singh, *et al.* (US 6,561,706, hereinafter referred to as Singh '706) further in view of Arita, *et al.* (US 6,690,949). It is respectfully requested that this rejection be withdrawn for at least the following reasons. Singh, Singh '706, and Arita, when taken alone or in combination, fail to disclose, teach, or suggest each and every element recited in the subject claims.

To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) *must teach or suggest all the claim limitations*. See MPEP §706.02(j). The *teaching or suggestion to make the claimed combination* and the reasonable expectation of success *must be found in the prior art and not based on the Applicant's disclosure*. See *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The subject claims generally relate to a system capable of detecting and mitigating line-edge roughness (LER) in a semiconductor photoresist while maintaining specified critical dimensions (CD). More specifically, independent claim 1 as amended (and similarly amended independent claims 10 and 17) recites *a monitoring component that monitors information associated with an original distance of a photoresist and line-*

edge roughness on a photoresist; a non-lithographic shrink component comprising at least one of a chemical component, a shrink enhancement component that shrinks a gate channel, or a thermal component that applies heat to the photoresist to a point for causing the photoresist to just enter a liquid phase to mitigate line-edge roughness, which in turn increases a distance between gates and decreases a thickness of the photoresist layer; and a trim etch component that is utilized to mitigate the increased distance between the gates by removing excess resist material resulting from the non-lithographic component so as to restore the original distance of the photoresist. Singh, Singh '706, and Arita, when taken alone or in combination, do not disclose, teach, or suggest such claimed aspects.

The system in Singh is generally capable of deriving information from a fabricated semiconductor in order to improve the fabrication process for subsequent semiconductors or features. (See col. 2, ll. 22-25). Singh adjusts *future* process parameters based on measured data of the pattern profiles. This is distinguishable from the subject invention in that the invention is concerned with mitigating line-edge roughness on an *ascertained* semiconductor and *restoring an original distance of an ascertained* semiconductor. Also, as contended by the Examiner in the First Office Action dated September 12, 2007, at page 3, nowhere in Singh is it taught or suggested that the subject claims provide a system or method for mitigating line-edge roughness using the non-lithographic technique. Accordingly, Singh does not teach or suggest all of the claim limitations of the subject invention.

Moreover, Singh '706 fails to cure the aforementioned deficiencies of Singh. Singh *et al.* '706 relates to a post manufacturing process system that controls *subsequent* processes for subsequently formed features based on collected data. Thus, Singh *et al.* '706 is able to cure subsequently formed features. On the contrary, the subject claims recite *restoring an original distance of the photoresist*. A trim etch component recited in the subject claims is utilized *to restore an original distance of an already fabricated feature*, not to control those subsequently formed features recited in Singh '706. Also, as contended by the Examiner in the First Office Action dated September 12, 2007, at page 4, Singh '706 does not disclose the mitigation of line-edge roughness recited in the

subject claims. Accordingly, Singh '706 does not teach or suggest all of the claim limitations of the subject invention.

Additionally, Arita, *et al.* fails to cure the aforementioned deficiencies of Singh and Singh '706. Arita is directed to a semiconductor apparatus fabrication method capable of effectively suppressing edge roughness when an extremely fine resist pattern is formed. The Examiner cites col. 4, lines 1-9 of Arita as allegedly disclosing the presently claimed "non-lithographic shrink component." Applicant's representative disagrees. These cited passages disclose that an extremely fine resist pattern is covered with a film whose heat-resistance temperature is higher than the softening temperature of the resist pattern. In this state, the resist pattern is heated at a temperature *higher than the softening temperature* of the resist pattern. This disclosure clearly teaches away from the subject invention, in which *no film layer is used*, and which includes *heating the photoresist to a point for causing the photoresist to just enter a liquid phase, which in turn increases a distance between gates and decreases a thickness of the photoresist layer*. Also, Arita, *et al.* fails to teach or suggest another non-lithographic shrink component such as *a shrink enhancement component that shrinks a gate channel* recited in the subject claims. Therefore, Arita fails to cure the aforementioned deficiencies of Singh and Singh '706.

Moreover, Kim *et al.*, in col. 3-16, discloses using RELACS process for correcting line-edge roughness. However, Kim *et al.* fails to teach or suggest *a shrink enhancement component that shrinks a gate channel* recited in the subject claims.

For at least the foregoing reasons, Singh, Singh '706, and Arita, when taken alone or in combination, fail to disclose, teach, or suggest each and every element as recited in independent claims 1, 10, and 17. More specifically, Singh '706 and Arita fail to make up for the deficiencies of Singh. Thus, rejection of these claims, as well as claims 3-8 and 18-23, which depend therefrom, should be withdrawn

II. Rejection of Claims 9 and 11-16 Under 35 U.S.C. §103(a)

Claims 9 and 11-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Singh in view of Singh '706 and Arita, as applied to claims 1, 3-8, 10, and 17-23 above, and further in view of Kim *et al.* (US 6,730,458). This rejection should be

withdrawn for at least the following reasons. Claims 9 and 15 have been cancelled. As discussed *supra*, Kim *et al.* fails to makeup for the aforementioned deficiencies of Singh, Singh '706, and Arita with respect to independent claims 1 and 10, from which claims 11-14 and 16 depend. Accordingly, this rejection should be withdrawn.

Conclusion

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP981US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,
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